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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

N/A

Office Action Summary	Application No.	Applicant(s)	
	10/754,501	LEE ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *8-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,7 and 12-14* is/are rejected.

7)☒ Claim(s) *2-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/25/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1-7 and 12-14, in the reply filed on 2/25/05 is acknowledged.

Drawings

2. The drawings are objected to because Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 7, the recitations "first signal" and "second signal" in this claim cause the claim to be indefinite because it is not clear if any one of the first and second signals is the same as "the signal output from the input part" recited in claim 1 (see lines 5 and 9 of claim

1), or the first and second signals are additional signals to "the signal output from the input part". If the first and second signals are additional signals to "the signal output from the input part", then it also would be misdescriptive because the input part (110, Figure 1) does not provide three different signals. Clarification and/or appropriate correction is required.

Also in claim 7, the recitation that "a third NMOS transistor having a drain connected to the drain of the first NMOS transistor" on lines 22-23 is indefinite because it is misdescriptive. Note that, as recited earlier in claim 7 that first NMOS having its gate receives a first signal output from the input part (see line 16) and that the second NMOS transistors having its gate receives a second signal output form the input part (see line 20) so the first NMOS transistor must be transistor 272 in Figure 2 of the invention, and the second NMOS transistor must be transistor 270 in Figure 2. Clearly, the drain of the third NMOS transistor (274, Figure 2) is connected to the drain of the NMOS transistor 270 (which is the second NMOS). Thus, it appears that "first" on line 23 must be changed to --second--. Clarification and/or appropriate correction is required.

Further, "the first" on line 25 is also misdescriptive for the similar reason as discussed since Figure 2 shows the inverter 276 having its input connected to the drain of the third NMOS 274 and the drain of NMOS 270 (which is the second NMOS). Thus, it appears that "first" on line 25 must be changed to --second--. Clarification and/or appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 6, 12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuda (JP 5-315931).

With respect to claim 1, Figure 1 of the Tsuda reference discloses a level shifter circuit, comprising: a power detection circuit (10) which generates a control signal (output of 10) in response to a first power supply voltage (Vcc, see Figure 4 and paragraph [0014] of the translation) and a second power supply voltage (Vdd, see Figure 4 and paragraph [0014] of the translation); and input circuit (2-3); an output circuit (QP1, Q1-Q4, QN1, 4); and input signal (T) and an output signal (output of inverter 4).

With respect to claim 6, Figure 1 shows the input part (2-3) including a first inverter (2) and second inverter (3).

With respect to claim 12, Figure 1 of the Tsuda reference discloses a level shifter circuit, comprising: a first power (Vcc); a second power (Vdd); an input circuit (2-3); an input signal (T); an output circuit (QP1, Q1-Q4, QN1, 4); and a detection circuit (10, also see Figure 4 and paragraph [0014] of the translation).

With respect to claim 14, Figure 1 shows the output circuit output circuit (QP1, Q1-Q4, QN1, 4) comprises an inverter (4) having an input that is grounded in response to the interruption detected by the detection circuit (because QN1 is ON so inverter 4 having its input connected to ground).

7. Claims 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Konishi (USP 6,373,285).

With respect to claim 12, Figure 1 of the Konishi reference discloses a level shifter circuit, comprising: a first power (70); a second power (80); an input circuit (1); an input signal (10); an output circuit (2); and a detection circuit (3).

With respect to claim 13, it is seen in the operation of the circuitry in Figure 1 of the Konishi reference that the interruption occurs during a power down operation mode (see abstract).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuda (JP 5-315931) in view of Konishi (USP 6,373,285).

With respect to claim 7, the circuitry in Figure 1 of the Tsuda reference discloses all of the limitations of this claim. The different between the prior art (Figure 1 of Tsuda) and the claimed invention is that the shifter unit of the output part of the prior art (i.e., QP1 and Q1-Q4 in Figure 1 of Tsuda) comprises first to third PMOS transistors and first and second NMOS transistors, while the shifter unit of the invention (262, 264, 266, 268, 280 and 270 in Figure 2 of the invention) comprises first to fourth PMOS transistors and first and second NMOS transistors. However, Figure 1 of the Konishi reference discloses a level shifter comprising an output part (2) wherein the shifter unit (14-19) of the output part (2) comprises first to fourth PMOS transistors and first and second NMOS transistors for the purpose of being secured to

prevent the flow of the through current from the second power supply to ground via the two NMOS transistors of the shifter unit of the output part during power down condition (see Col. 9, lines 5-24, Konishi). Thus, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 1 of the Konishi reference by replacing the shifter unit (QP1, Q1-Q4) in Figure 1 of the Tsuda reference with the specific shifter unit (14-19) in Figure 1 of the Konishi reference for the purpose of being secured to prevent the flow of the through current from the second power supply to ground during power down condition, and thus the overall power consumption of the circuitry is reduced. Thus, this modification meets all the limitations of claims 7 as that the output part includes first to fourth PMOS transistors, first to third NMOS transistors and an inverter as recited in claim 7 since the structure of the of the output part in this combination/modification is substantially similar as that of the invention. In particularly, by using specific shifter unit (14-19) in Figure 1 of Konishi to replace the shifter unit (QP1 and Q1-Q4) in Figure 1 of Tsuda, then the output part in the above discussed modified/combined comprises: a first PMOS (15, Figure 1 of Konishi), a second PMOS (14, Figure 1 of Konishi), a third PMOS (17, Figure 1 of Konishi), a fourth PMOS (16, Figure 1 of Konishi), a first NMOS transistor (19, Figure 1 of Konishi), a second NMOS (18, Figure 1 of Konishi), a third NMOS (QN1, Figure 1 of Tsuda) and an inverter (4, Figure 1 of Tsuda).

Allowable Subject Matter

10. Claims 2-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 28, 2005

LONG NGUYEN
PRIMARY EXAMINER